WHAT IS CLAIMED IS:

1. An apparatus for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the apparatus comprising:

a control circuit adapted to provide a control signal; and

a signal generator adapted to

receive a first clock signal comprising k pulses each having a first duration,

change the duration of each of m of the pulses to a second duration in response to the control signal, wherein m < k and the second duration is not substantially equal to the first duration, to produce a second clock signal, and

apply the second clock signal to the clock inputs of the plurality of clocked storage elements.

2. The apparatus of claim 1, further comprising:

a clock circuit adapted to provide the clock signal.

3. The apparatus of claim 2, further comprising:

a measurement circuit adapted to measure a signal generated by the integrated circuit in response to the second clock signal.

4. The apparatus of claim 3, further comprising:

a comparison circuit adapted to compare the signal generated by the integrated circuit to a predicted signal to obtain a test result.

5. The apparatus of claim 4, further comprising:

an analysis circuit adapted to identify one of the signal paths as flawed based on the test result.

6. The apparatus of claim 5:

wherein the signal generator is further adapted to

change the duration of every nth pulse of the signal to the second duration to produce the second clock signal; and

successively apply the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal.

7. The apparatus of claim 6, wherein n = 2.

8. The apparatus of claim 7:

wherein the comparison circuit is further adapted to compare the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein the analysis circuit identifies at least one of the n different predetermined phases as a failure phase.

9. The apparatus of claim 8:

wherein the signal generator is further adapted to apply the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of a test time;

wherein the comparison circuit is further adapted to compare values stored in the clocked storage elements to predicted values; and

wherein the signal generator is further adapted to apply the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements are not equal to the predicted values.

10. The apparatus of claim 9:

wherein the comparison circuit is further adapted to compare a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

wherein the analysis circuit is further adapted to identify as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

11. The apparatus of claim 10:

wherein the comparison circuit is further adapted to compare the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

wherein the analysis circuit is further adapted to identify as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

12. The apparatus of claim 3:

wherein the one of the clocked storage elements is part of a scan chain; and

wherein the measurement circuit is further adapted to shift the contents of the scan chain from the integrated circuit to the measurement circuit.

13. An apparatus for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the apparatus comprising:

control means for providing a control signal; and

signal generator means for

receiving a first clock signal comprising k pulses each having a first duration,

changing the duration of each of m of the pulses to a second duration in response to the control signal, wherein $m < k$ and the second duration is not substantially equal to the first duration, to produce a second clock signal, and

applying the second clock signal to the clock inputs of the plurality of clocked storage elements.

14. The apparatus of claim 13, further comprising:

clock means for providing the clock signal.

15. The apparatus of claim 14, further comprising:

measurement means for measuring a signal generated by the integrated circuit in response to the second clock signal.

16. The apparatus of claim 15, further comprising:

comparison means for comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result.

17. The apparatus of claim 16, further comprising:

analysis means for identifying one of the signal paths as flawed based on the test result.

18. The apparatus of claim 17, wherein the signal generator means comprises:

means for changing the duration of every nth pulse of the signal to the second duration to produce the second clock signal; and

means for successively applying the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal.

19. The apparatus of claim 18, wherein n = 2.

20. The apparatus of claim 19:

wherein the comparison means comprises means for comparing the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein the analysis means comprises means for identifying at least one of the n different predetermined phases as a failure phase.

21. The apparatus of claim 20:

wherein the signal generator means further comprises means for applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of a test time;

wherein the comparison means further comprises means for comparing values stored in the clocked storage elements to predicted values; and

wherein the signal generator means further comprises means for applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements are not equal to the predicted values.

22. The apparatus of claim 21:

wherein the comparison means further comprises means for comparing a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

wherein the analysis means further comprises means for identifying as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

23. The apparatus of claim 22:

wherein the comparison means further comprises means for comparing the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

wherein the analysis circuit means further comprises means for identifying as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

24. The apparatus of claim 15:

wherein the one of the clocked storage elements is part of a scan chain; and

wherein the measurement means further comprises means for shifting the contents of the scan chain from the integrated circuit to the measurement circuit.

25. A method for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the method comprising:

receiving a first clock signal comprising k pulses each having a first duration;

changing the duration of each of m of the pulses to a second duration in response to the control signal, wherein $m < k$ and the second duration is not substantially equal to the first duration, to produce a second clock signal; and

applying the second clock signal to clock inputs of a plurality of clocked storage elements interconnected by a plurality of signal paths in a circuit.

26. The method of claim 25, further comprising:

measuring a signal generated by the integrated circuit in response to the second clock signal.

27. The method of claim 26, further comprising:

comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result.

28. The method of claim 27, further comprising:

identifying one of the signal paths as flawed based on the test result.

29. The method of claim 28:

wherein changing the duration of m of the pulses comprises changing the duration of every nth pulse of the signal to the second duration to produce the second clock signal; and

wherein applying the second clock signal to the clock inputs of the clocked storage elements comprises successively applying the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of

the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal.

30. The method of claim 29, wherein n = 2.

31. The method of claim 29:

wherein comparing the signal generated by the integrated circuit to the predicted signal comprises comparing the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein identifying one of the signal paths as flawed comprises identifying at least one of the n different predetermined phases as a failure phase.

32. The method of claim 31, wherein identifying one of the signal paths as flawed further comprises:

searching a predetermined test time, comprising

(a) applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of the test time,

(b) comparing values stored in the clocked storage elements to predicted values, and

(c) applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements in step (b) are not equal to the predicted values.

33. The method of claim 32, wherein identifying one of the signal paths as flawed further comprises:

comparing a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

34. The method of claim 33, wherein identifying as flawed one of the signal paths further comprises:

comparing the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

35. The method of claim 26, wherein the one of the clocked storage elements is part of a scan chain, further comprising:

shifting the contents of the scan chain from the integrated circuit to the measurement circuit.

36. A computer program embodying instructions executable by a computer to perform a method for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the method comprising:

receiving a first clock signal comprising k pulses each having a first duration;

changing the duration of each of m of the pulses to a second duration in response to the control signal, wherein $m < k$ and the second duration is not substantially equal to the first duration, to produce a second clock signal; and

applying the second clock signal to clock inputs of a plurality of clocked storage elements interconnected by a plurality of signal paths in a circuit.

37. The computer program of claim 36, wherein the method further comprises:

measuring a signal generated by the integrated circuit in response to the second clock signal.

38. The computer program of claim 37, wherein the method further comprises:

comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result.

39. The computer program of claim 38, wherein the method further comprises:

identifying one of the signal paths as flawed based on the test result.

40. The computer program of claim 39:

wherein changing the duration of m of the pulses comprises changing the duration of every nth pulse of the signal to the second duration to produce the second clock signal; and

wherein applying the second clock signal to the clock inputs of the clocked storage elements comprises successively applying the second clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the second clock signal.

41. The computer program of claim 40, wherein n = 1.

42. The computer program of claim 40:

wherein comparing the signal generated by the integrated circuit to the predicted signal comprises comparing the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein identifying one of the signal paths as flawed comprises identifying at least one of the n different predetermined phases as a failure phase.

43. The computer program of claim 42, wherein identifying one of the signal paths as flawed further comprises:

searching a predetermined test time, comprising

(a) applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of the test time,

(b) comparing values stored in the clocked storage elements to predicted values, and

(c) applying the failure phase of the second clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements in step (b) are not equal to the predicted values.

44. The computer program of claim 43, wherein identifying one of the signal paths as flawed further comprises:

comparing a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

45. The computer program of claim 44, wherein identifying as flawed one of the signal paths further comprises:

comparing the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

46. The computer program of claim 37, wherein the one of the clocked storage elements is part of a scan chain, and wherein the method further comprises:

shifting the contents of the scan chain from the integrated circuit to the measurement circuit.

47. An apparatus for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the apparatus comprising:

a control circuit adapted to provide a control signal; and

a signal generator adapted to

produce a clock signal comprising j pulses each having the first duration and m pulses having a second duration in response to the control signal, wherein $k = m + j$, and wherein the second duration is not substantially equal to the first duration, to produce a clock signal, and

apply the clock signal to the clock inputs of the plurality of clocked storage elements.

48. The apparatus of claim 47, further comprising:

a measurement circuit adapted to measure a signal generated by the integrated circuit in response to the clock signal.

49. The apparatus of claim 48, further comprising:

a comparison circuit adapted to compare the signal generated by the integrated circuit to a predicted signal to obtain a test result.

50. The apparatus of claim 49, further comprising:

an analysis circuit adapted to identify one of the signal paths as flawed based on the test result.

51. The apparatus of claim 50:

wherein $m = nj$ and every pulse of the clock signal having the first duration is followed by n pulses having the second duration; and

wherein the signal generator is further adapted to successively apply the clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the clock signal.

52. The apparatus of claim 51, wherein n = 2.

53. The apparatus of claim 52:

wherein the comparison circuit is further adapted to compare the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein the analysis circuit identifies at least one of the n different predetermined phases as a failure phase.

54. The apparatus of claim 53:

wherein the signal generator is further adapted to apply the failure phase of the clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of a test time;

wherein the comparison circuit is further adapted to compare values stored in the clocked storage elements to predicted values; and

wherein the signal generator is further adapted to apply the failure phase of the clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements are not equal to the predicted values.

55. The apparatus of claim 54:

wherein the comparison circuit is further adapted to compare a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

wherein the analysis circuit is further adapted to identify as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

56. The apparatus of claim 55:

wherein the comparison circuit is further adapted to compare the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

wherein the analysis circuit is further adapted to identify as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

57. The apparatus of claim 48:

wherein the one of the clocked storage elements is part of a scan chain; and

wherein the measurement circuit is further adapted to shift the contents of the scan chain from the integrated circuit to the measurement circuit.

58. An apparatus for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the apparatus comprising:

control means for providing a control signal; and

signal generator means for

producing a clock signal comprising j pulses each having the first duration and m pulses having a second duration in response to the control signal, wherein k = m + j, and wherein the second duration is not substantially equal to the first duration, to produce a clock signal, and

applying the clock signal to the clock inputs of the plurality of clocked storage elements.

59. The apparatus of claim 58, further comprising:

measurement means for measuring a signal generated by the integrated circuit in response to the clock signal.

60. The apparatus of claim 59, further comprising:

comparison means for comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result.

61. The apparatus of claim 60, further comprising:

analysis means for identifying one of the signal paths as flawed based on the test result.

62. The apparatus of claim 61:

wherein m = nj and every pulse of the clock signal having the first duration is followed by n pulses having the second duration; and

wherein the signal generator comprises means for successively applying the clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the clock signal.

63. The apparatus of claim 62, wherein n = 2.

64. The apparatus of claim 63:

wherein the comparison means comprises means for comparing the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein the analysis means comprises means for identifying at least one of the n different predetermined phases as a failure phase.

65. The apparatus of claim 64:

wherein the signal generator means further comprises means for applying the failure phase of the clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of a test time;

wherein the comparison means further comprises means for comparing values stored in the clocked storage elements to predicted values; and

wherein the signal generator means further comprises means for applying the failure phase of the clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements are not equal to the predicted values.

66. The apparatus of claim 65:

wherein the comparison means further comprises means for comparing a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

wherein the analysis means further comprises means for identifying as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

67. The apparatus of claim 66:

wherein the comparison means further comprises means for comparing the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

wherein the analysis means further comprises means for identifying as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

68. The apparatus of claim 59:

wherein the one of the clocked storage elements is part of a scan chain; and

wherein the measurement means further comprises means for shifting the contents of the scan chain from the integrated circuit to the measurement circuit.

69. A method for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the method comprising:

receiving a control signal;

producing a clock signal comprising k pulses including j pulses each having a first duration and m pulses having a second duration in response to the control signal, wherein $k = m + j$, and wherein the second duration is not substantially equal to the first duration; and

applying the clock signal to the clock inputs of the plurality of clocked storage elements.

70. The method of claim 69, further comprising:

measuring a signal generated by the integrated circuit in response to the clock signal.

71. The method of claim 70, further comprising:

comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result.

72. The method of claim 71, further comprising:

identifying one of the signal paths as flawed based on the test result.

73. The method of claim 72:

wherein $m = nj$ and every pulse of the clock signal having the first duration is followed by n pulses having the second duration; and

wherein applying the clock signal to the clock inputs of the clocked storage elements comprises successively applying the clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the clock signal.

74. The method of claim 73, wherein $n = 2$.

75. The method of claim 73:

wherein comparing the signal generated by the integrated circuit to the predicted signal comprises comparing the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein identifying one of the signal paths as flawed comprises identifying at least one of the n different predetermined phases as a failure phase.

76. The method of claim 75, wherein identifying one of the signal paths as flawed further comprises:

searching a predetermined test time, comprising

(a) applying the failure phase of the clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of the test time,

(b) comparing values stored in the clocked storage elements to predicted values, and

(c) applying the failure phase of the clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements in step (b) are not equal to the predicted values.

77. The method of claim 76, wherein identifying one of the signal paths as flawed further comprises:

comparing a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

78. The method of claim 77, wherein identifying as flawed one of the signal paths further comprises:

comparing the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the

clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

79. The method of claim 70, wherein the one of the clocked storage elements is part of a scan chain, further comprising:

shifting the contents of the scan chain from the integrated circuit to the measurement circuit.

80. A computer program embodying instructions executable by a computer to perform a method for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the method comprising:

receiving a control signal;

producing a clock signal comprising k pulses including j pulses each having a first duration and m pulses having a second duration in response to the control signal, wherein k = m + j, and wherein the second duration is not substantially equal to the first duration; and

applying the clock signal to the clock inputs of the plurality of clocked storage elements.

81. The computer program of claim 80, wherein the method further comprises:

measuring a signal generated by the integrated circuit in response to the clock signal.

82. The computer program of claim 81, wherein the method further comprises:

comparing the signal generated by the integrated circuit to a predicted signal to obtain a test result.

83. The computer program of claim 82, wherein the method further comprises:

identifying one of the signal paths as flawed based on the test result.

84. The computer program of claim 83:

wherein m = nj and every pulse of the clock signal having the first duration is followed by n pulses having the second duration; and

wherein applying the clock signal to the clock inputs of the clocked storage elements comprises successively applying the clock signal at n different predetermined phases to the clock inputs of the clocked storage elements, wherein each of the predetermined phases is offset from another of the predetermined phases by a period of the clock signal.

85. The computer program of claim 84, wherein n = 2.

86. The computer program of claim 84:

wherein comparing the signal generated by the integrated circuit to the predicted signal comprises comparing the signal generated by the integrated circuit to the predicted signal n times, each time corresponding to one of the n different predetermined phases; and

wherein identifying one of the signal paths as flawed comprises identifying at least one of the n different predetermined phases as a failure phase.

87. The computer program of claim 86, wherein identifying one of the signal paths as flawed further comprises:

searching a predetermined test time, comprising

(a) applying the failure phase of the clock signal to the clock inputs of the clocked storage elements during a first predetermined portion of the test time,

(b) comparing values stored in the clocked storage elements to predicted values, and

(c) applying the failure phase of the clock signal to the clock inputs of the clocked storage elements during a second predetermined portion of the first predetermined portion of the test time when the values stored in the clocked storage elements in step (b) are not equal to the predicted values.

88. The computer program of claim 87, wherein identifying one of the signal paths as flawed further comprises:

comparing a value stored by one of the clocked storage elements to a corresponding one of the predicted values; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements when the value stored by the one of the clocked storage elements is not equal to the corresponding one of the predicted values.

89. The computer program of claim 88, wherein identifying as flawed one of the signal paths further comprises:

comparing the value stored by a further one of the clocked storage elements to a further corresponding one of the predicted values, wherein the value stored by the one of the clocked storage elements is a function of the value stored by the further one of the clocked storage elements; and

identifying as flawed one of the signal paths connected to the one of the clocked storage elements and the further one of the clocked storage elements when the value stored by the further one of the clocked storage elements is not equal to the further corresponding one of the predicted values.

90. The computer program of claim 81, wherein the one of the clocked storage elements is part of a scan chain, wherein the method further comprises:

shifting the contents of the scan chain from the integrated circuit to the measurement circuit.